

CONSTRUCTION OF A CURRENT-FED PUSH-PULL CONVERTER: PRACTICAL CONSIDERATIONS

CONSTRUCCIÓN DE UN CONVERTIDOR PUSH-PULL ALIMENTADO EN CORRIENTE: CONSIDERACIONES PRÁCTICAS

Ibsan Ulises Castillo Zamora

Tecnológico Nacional de México en Celaya
ibsancastillo@gmail.com

Adyr Andrés Estévez de Bén

Tecnológico Nacional de México en Celaya
adyrandres@gmail.com

Alfredo Alvarez Díaz Comas

Tecnológico Nacional de México en Celaya
alfredoadc92@gmail.com

Juan José Elías Rodríguez Segura

Tecnológico Nacional de México en Celaya
ejjrseg@gmail.com

Abstract

This paper deals with the construction considerations for a current-fed push-pull converter. It is common to find sufficient bibliography about the operation principle of a current fed push-pull converter and the size of its elements. However, when building a prototype issues that were not considered and documented arise. The aim of this paper is to expose the considerations to consider when a current-fed push-pull converter is implemented. These considerations were the main insight to build a 300 W and 48 voltage output prototype, powered by the grid.

Keywords: Push-Pull, converter, construction, current-fed.

Resumen

En este trabajo se abordan los aspectos a tener en consideración para la construcción de un convertidor Push-Pull alimentado en corriente. Cuando se va a implementar un convertidor es común encontrar suficiente bibliografía sobre el funcionamiento del convertidor Push-Pull alimentado en corriente y el

dimensionamiento de sus elementos. Sin embargo, cuando en la etapa de implementación física surgen ciertos retos que no se consideran en el diseño y de los cuales no existe abundante literatura. El propósito de este trabajo es exponer en un documento las consideraciones a tener en cuenta cuando se implementa un convertidor push-pull alimentado en corriente. Estas consideraciones fueron clave para realizar un prototipo de 300 W energizado desde la red eléctrica y con 48 V de tensión en su salida.

Palabras claves: *convertidor, push-pull, construcción, alimentado en corriente.*

1. Introduction

Push-pull converters are widely used for their advantages over other converters. Their main characteristics are discussed in [1, 2]. It is important to highlight the isolation between the input and output stages, the removal of the isolated sources for the drivers of the MOSFETs, the non-pulsating output current and the small transformer, to mention just a few. Moreover, the current-fed configuration makes an inherent protection against short circuits at the output for the converter.

The construction process of a circuit begins with the design and parameters of its elements. Typically, there are many references in this stage of the project for the current fed push pull prototype [3,4,5,6], however, there are many practical aspects that need to be considered to achieve the proposed operation of the circuit. It is well noted that there is not a lot of bibliography that allow a transition among the design and construction phases.

Therefore, the purpose of this paper is to resume in a document all the procedures that are needed for the satisfactory construction of the converter starting from the design until the implementation. This article does not include all the issues that may be confronted, although it intends to be a guide to address this type of converters configuration. These considerations are considered for the development of a prototype that is grid-connected, as input power supply, and presents a 48 V output with a nominal power of 300 W.

From the construction of the circuit, important results were obtained and some of them must be highlighted; removing spikes in MOSFETs and obtaining a permissible

V_{ds} signal with an auxiliary snubber circuit, decreasing the noise interferences in the printed circuit board (PCB) due to a good design of the circuitry, eradicating the noise in the output signal due to MOSFETs commutations by the output filter and performing of the magnetics elements needed for the system.

The design procedure for a current-fed push-pull converter is described in [6]. Furthermore, there are some aspects that may be of interest for the control loop, such as the transfer function of the system. Even though, practical aspects for the elaboration of the converter were not discussed.

2. Development

The work starts by establishing the theoretical bases that govern the behavior of the device. In [7] it is discussed the push-pull converter's characteristics in the steady state. The operation of the studied converter was defined in continuous conduction mode (CCM). Figure 1 shows the schematic design of the current fed push-pull converter. It has a transformer with a central tap. The basic operation of the push-pull converter is described in the Operation Section of [6].

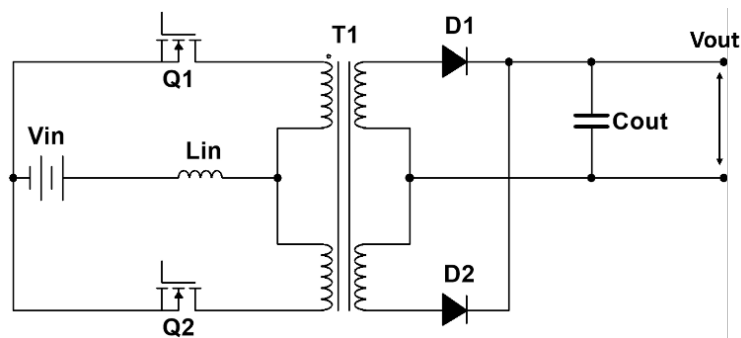


Figure 1 Current-fed push-pull converter.

The design equations use are shown in [6]. The design specifications are the next values:

- Input voltage: $V_{in} = 180 \text{ V} \pm 10 \text{ V}$.
- Output voltage: $V_{out} = 48 \text{ V}$.
- Nominal output power: $P_{out} = 300 \text{ W}$.
- Switching frequency: $f_s = 100 \text{ kHz}$.

Table 1 shows the results obtained from the design requirements.

Table 1 Design parameters for the push-pull converter.

Duty cycle	
$D_{\text{máx}}, D_{\text{mín}}$	0.57, 0.54
Inductor	
$L_{\text{in min}}$	469 μH
Transformer	
N, N_p, N_s	4.375, 24.4, 5.59
Output capacitor	
C_{out}	3.1 μF
MOSFETs	
$V_{\text{DS MÁX}}$	800 v
$I_{\text{DS MÁX}}$	4.47 A
Diodes	
$I_{\text{D MÁX}}$	19.56 A

Where: $D_{\text{MÁX}}$: Maximum duty cycle, $D_{\text{MÍN}}$: Minimum duty cycle, $L_{\text{IN MÍN}}$: Minimum inductance permissible value for the input inductor, N : turns ratio of transformer, N_p : Number of turns in the primary winding, N_s : Number of turns in the secondary winding.

Input stage

The power supply for a current fed push-pull converter must be a DC source. In this application was the grid with a rectification stage to obtain a DC input voltage. This stage contains a fuse and varistor for current and voltage spikes protection respectively, EMI filter and a full wave rectifier.

The fuse selection depends of application current and voltage. For the input stage of the system a 1.76 A is selected. The cut current of the device is selected for 3 A. Moreover, the varistor value was calculated for a 20% of increase in the input voltage: 150 V. With these elements the system is protected against overcurrent and overvoltage.

There is also the necessity to not inject high-frequency parasites harmonics due the switching of the MOSFETs into the grid, furthermore it is necessary to mitigate the unwanted effects coming from the grid itself too. There are several procedures for

the design of the EMI filter, in [8] the most commonly used EMI filters are listed. In this application the values calculated were: $C1 = 0.1 \mu F$, $C2 = 0.1 \mu F$, $L1 = 9 mH$, $L2 = 9 mH$. Output Capacitor ($C3$ in figure 2) is an important element to settle the input voltage of the converter. With a permissible ripple of 5% of the nominal voltage value, then V_r is equal to 8.5 V. So, the capacitance is given by equation 1.

$$C_3 = \frac{I}{V_r * 2 * f} = \frac{1.76}{8.5 * 120} = 1.725 mF \quad (1)$$

Where: I: Current of the input stage, V_r : Ripple voltage, f: Grid frequency.

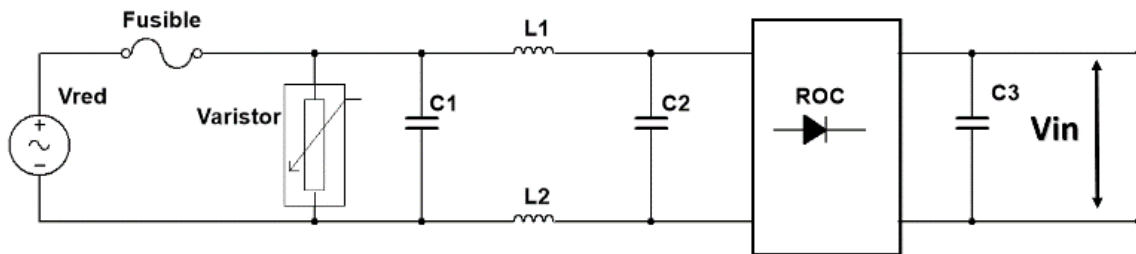


Figure 2 Input stage.

Magnetic Devices

The inductor, as well as the transformer, has design and construction considerations. The same considerations, for both transformer and inductor, need to be done to avoid saturation and to decrease the losses. The inductor design is made by following the methodology for inductor with ETD cores shown in [9]. With this procedure an ETD39 core is selected, a 0.43 mm^2 area for the wire, 24 turns and an air gap of 0.2 mm.

One of the main concerns in the isolated converters, like the push-pull, is the transformer. There are some issues that need to be avoid improving the correct performance of the transformer. Saturation is one of the main problems that may be present in the transformer, as well as the core and winding losses.

The first consideration to make in the transformer design is to select an operation frequency. By selecting a correct frequency, the size of the transformer can be smaller and minimize the losses. The higher the frequency the higher the saturation level can be achieved and the smaller size of the core, nevertheless the tradeoff

provokes in the system more winding losses, due to the skin effect, and more commutation losses in the switching devices.

The overall frequency of the converter is not up to the transformer itself, as mentioned before if the frequency increases then the winding, core and switching losses increase as well. Therefore, it is of special consideration to select the operation frequency considering the losses in the transformer and the switches. With a 100 kHz frequency, the wire to avoid the skin effect (AWG 30) is easily found for buying. At higher frequencies the depth of the skin effect shown in equation 2 decrease. The effect of the skin effect can be mitigated by using litz wire, although it is difficult to buy in small quantities.

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \quad (2)$$

Another consideration must be done for the proximity effect. The winding conductors induce eddy currents in adjacent conductors, altering the overall distribution of current flowing through them. The result is that the current is concentrated in the areas of the conductor farthest away from nearby conductors carrying current in the same direction. To avoid the proximity effect an interleaving configuration of windings is recommended as shown in figure 3. With this arrangement the magnetic flux of nearby conductors cancel each other because the currents are induced in opposite direction.

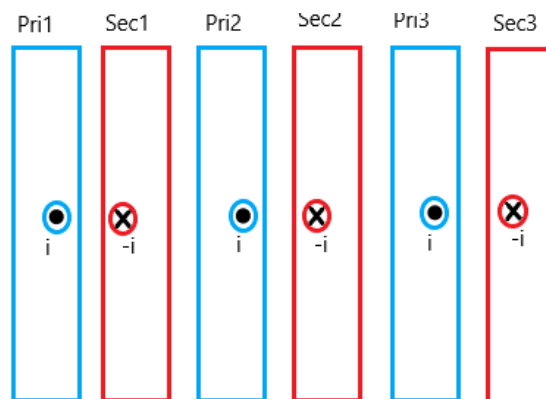


Figure 3 Interleaving configuration of primary and secondary winding.

The design procedure of the transformer is described in [6]. This design methodology is a good approach for the transformer development. The use of a finite element analysis tool is important for a precise description of the transformer performance. With this software the response of the transformer is predicted with the considerations that were made. For the development of this work the finite element analysis tool used is ANSYS, the model and the results of the simulation are shown in figures 4 and 5. The model has winding simplification to get a faster solution time and requires less computational resources as stated in [10].

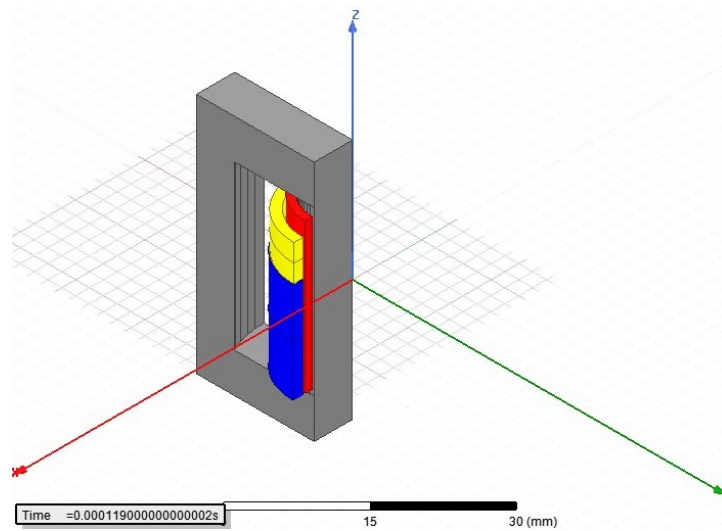


Figure 4 Finite element analysis (FEA) model of the transformer used in ANSYS.

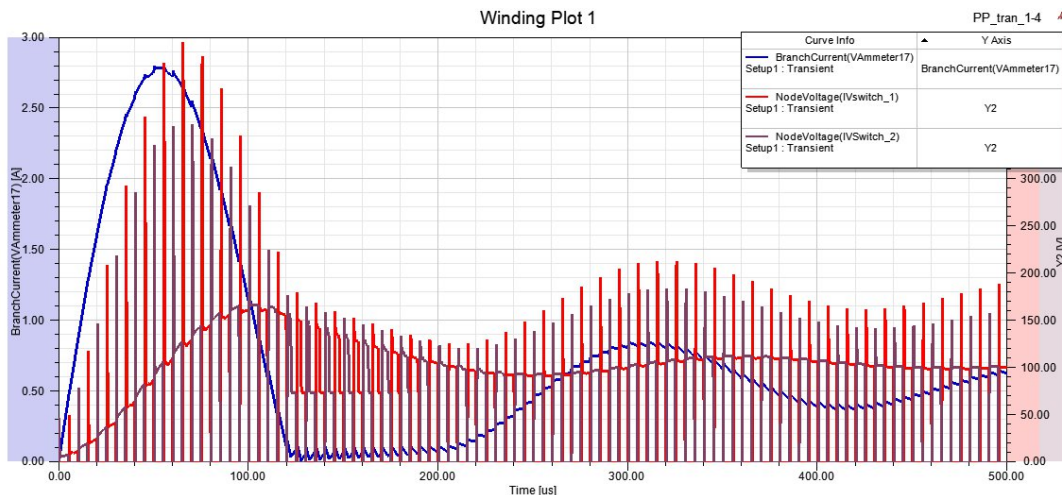


Figure 5 Push-pull transformer FEA results (Inductor current in blue, Switches voltages V_{DS} in brown and red).

Several core models can be used for the transformer construction. The decision is taken from the designer expertise and the resources available. This does not compromise the system functionality, nonetheless the chosen model must be within the calculated parameters. Finally, the windings of the transformer need to be balanced and with the correct dots connections of each coil. A transformer is balanced if the two windings has the same inductance, so it is necessary to modify the turns until it is accomplished for each winding. Once the transformer is balanced it is necessary to check the connections. To achieve this, the inductance from end to end of the winding is measured. If the value corresponds to two times the sum of both coil inductances then it is well connected, on the contrary it means that the coils are not properly connected.

Semiconductor devices

The MOSFETs need to be oversized in the voltage across the drain-source by a safety factor of 2, as stated in [6]. The SPI08N80C3 present a maximum V_{DS} of 800 V, so it is suitable for this application. The heat sink is calculated and the thermal resistance of 0.1553 ° C / W maximum is given.

The signal V_{DS} normally presents spikes due the leakage inductance of the transformer [10]. This overvoltage can damage the device even if it is oversized. To avoid this problem, the use of snubbers circuits is proposed. These systems consist of a capacitor and a resistor in shunt with the MOSFET to protect it. The snubber circuit can absorb the power when overstep a safety defined voltage.

The snubbers design is carried out starting with the measurement of the spikes resonance frequency. Then it is necessary to add a shunt capacitor across the drain-source of the MOSFET and adjust the value of this capacitor until the frequency of the spike resonance is reduced by a factor of two. The value of this resulting capacitor will be three times the value of the parasitic capacitance that is creating the voltage spikes. Because the parasitic capacitance is known (100 pF), the parasitic inductance can be determined using equation 3.

$$L_P = \frac{1}{(2\pi * f_r)^2 * C_p} = \frac{1}{(2\pi * 1.9 \text{ kHz})^2 * 100 \text{ pF}} = 67 \text{ mH} \quad (3)$$

Where: L_P : Parasitic inductance, C_P : Parasitic capacitance, f_r : Resonance frequency. Now that both the parasitic capacitance and inductance are known, the characteristic impedance of the resonance can be determined using equation 4.

$$Z = \sqrt{\frac{L_P}{C_P}} = 820 \Omega \quad (4)$$

The resistor in the RC snubber circuit should match the value of the characteristic impedance, and the capacitor should be sized between four and ten times the parasitic capacitance. The use of larger capacitors slightly reduces the voltage overshoot at the expense of greater power dissipation and less inverter efficiency. In this application the values selected were: $R = 820 \Omega$, $C = 1000 \text{ pF}$ (figure 5).

Output filter

Switched DC-DC power supplies have an inherent output noise with oscillations at the switching frequency. The noise can be avoided with an appropriate LC filter at the output as shown in figure 6.

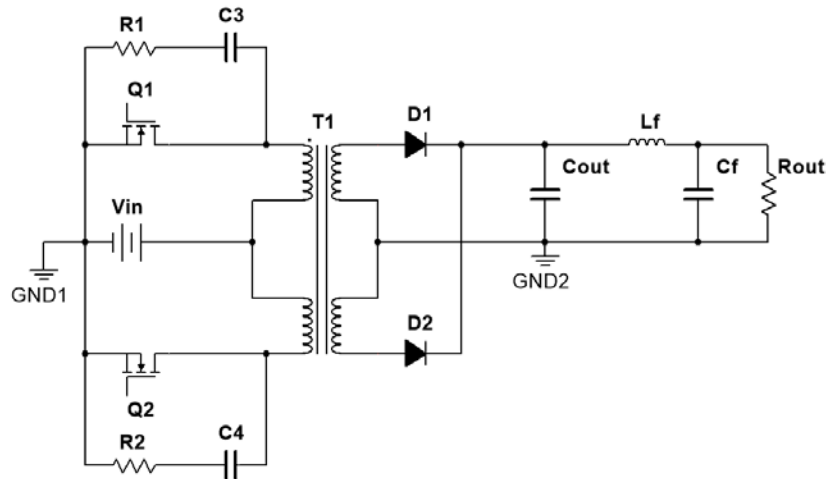


Figure 6 Output filter and snubber ubicacion.

These elements are calculated starting from a cutoff frequency and the load resistance. In this case a cutoff frequency to the half of the switching frequency is set, 50 kHz. In addition, the output resistance of the device is determined to

guarantee an output power of 300 W: $R_{out} = 6.8 \Omega$. Then the values of the filters elements are calculated in equations 5 and 6.

$$L_f = \frac{R_{out} * \sqrt{2}}{2 * \pi * f_0} = \frac{7.5 * \sqrt{2}}{2 * \pi * 50000} = 33.76 \mu H \quad (5)$$

$$C_f = \frac{1}{2 * \pi * f_0 * R_{out} * \sqrt{2}} = \frac{1}{2 * \pi * 50000 * 7.5 * \sqrt{2}} = 300 \text{ nF} \quad (6)$$

TL494 y TLP250

The converter operation is regulated through the integrated circuit (IC) TL494. This device is implemented in its push-pull mode. In this mode, outputs 8 and 11 are complementary. Furthermore, the duty cycle is limited from 50 to 100%. This duty cycle is set in pin 3, in this application it is ground reference due to the average duty cycle is 0.559. Then the operation is assured close to the operating point. The TL494 configuration is shown in figure 7.

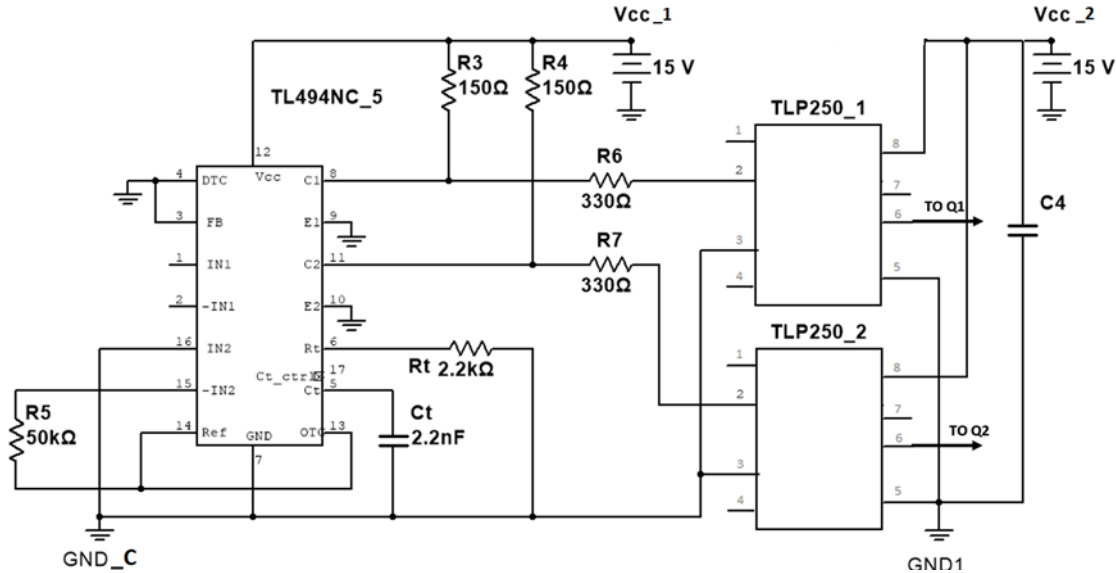


Figure 7 TL494 connections.

The R_T and C_T values were obtained from equation 7. The value of the resistor was set to 2.2 k Ω , resulting in a capacitor value of 2.2 nF.

$$f_{osc} = \frac{1.1}{2 * C_T * R_T} \quad (7)$$

$$C_T = \frac{1.1}{2 * 2.2 \text{ k}\Omega * 100 \text{ kHz}}$$

$$C_T = 2.5 \text{ nF} \approx 2.2 \text{ nF}$$

It is important to note that the control ground represented in the previous figure is independent from GND1 and GND2. The output signals (pins 8 and 11), were connected to the input of the optocouplers through a current limiter resistor. In this case, the TLP250 optocouplers are selected. This device provides the needed V_{GS} for the activation of the MOSFETs at the switching frequency of the application. The decoupling capacitor C_4 was set to 100 μF .

Initials conditions in power supply of the control circuit

In the projection of this converter is included a self-powered stage to guarantee the initials conditions in the power supply of the control circuit. This is useful for the start-up of the circuit, and there is no power in the auxiliary windings. This is accomplished by a voltage divider as shown in figure 8. First it is necessary to compute the value of the equivalent resistance of the control circuits. With an external power supply, it is measured for 15 V and 150 mA. Then the equivalent resistance is calculated as R_{10} in equation 8. Then the value of R_9 is set to 1 k Ω , and is calculated the value of R_8 to assure 15 V in V_a . This is accomplished by clearing R_8 from equation 9 (equation of the voltage divider).

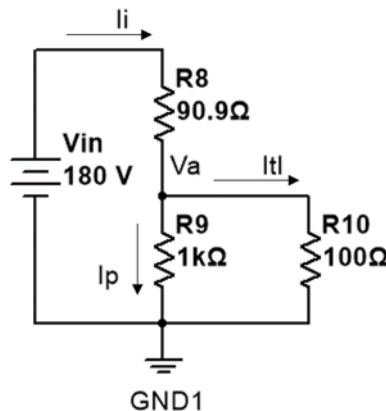


Figure 8 Voltage divider.

$$R_{10} = \frac{V_A}{I_{TL}} = \frac{15 V}{0.150 A} = 100 \Omega \quad (8)$$

$$V_A = \frac{R_9 // R_{10}}{R_8 + R_9 // R_{10}} * V_{CC} \quad (9)$$

$$R_8 = \frac{V_{CC}}{V_A} * \frac{R_9}{R_{10}} - \frac{R_9}{R_{10}} = \frac{180 V}{15 V} * 90.9 \Omega - 90.9 \Omega = 999.9 \Omega \approx 1 k\Omega$$

PCB design considerations

To avoid the noise in the circuits it is very important a good design of the PCB. These are the main considerations in this topic: the control ground and the output ground can only be connected in one point, the control signals can't flow beneath the transformer, the MOSFETs, drivers and transformer must be close to each other and with the shortest path possible, the power lines must be parallels through the board.

3. Results

In order to verify the correct operation of the converter, different tests are carried out to check its performance. The first thing that must be verified is the control stage. The TL494 was configured in push-pull mode and the switching frequency of 100 kHz was achieved with values of $R_T = 2.2 k\Omega$ and $C_T = 2.2 nF$. The waveform obtained for V_{GS} is shown in figure 9. It can be seen that the signal is symmetric. In addition, there is a time when both switches are on so the circuit is working in overlapping mode. This is necessary because the converter is current-fed, otherwise dead time would be necessary.

The next step will be to check the VDS signal. As explained in previous section it is important to consider the oscillations that will be obtained, so the nominal voltage in the power stage should not be used in calculates. For this experiment the circuit was energized with 60 V. The signal obtained is shown in figure 10. The surges can reach values greater than twice the expected signal and with a lot of oscillations. This waveform is inadmissible, and for so the snubber circuit is designed.

The snubber is designed as described in the previous section. The values of the resistance and the capacitor used were 820 Ω and 1000 pF respectively. The effect

of the snubber can be seen in figure 11. It can be appreciated that the oscillations practically disappear. Furthermore, voltage overshoot was significantly reduced. In this way, the switching device is protected and a valid signal is obtained.



Figure 9 PWM control signals from the TL494 circuit.

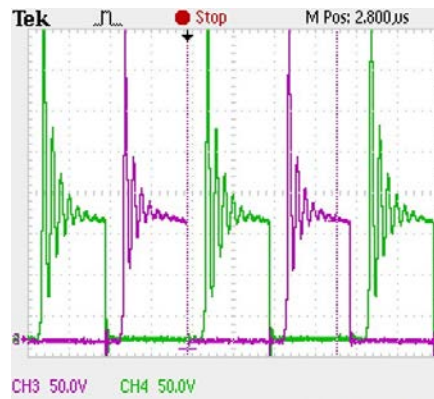


Figure 10 Voltages spikes in V_{DS} .

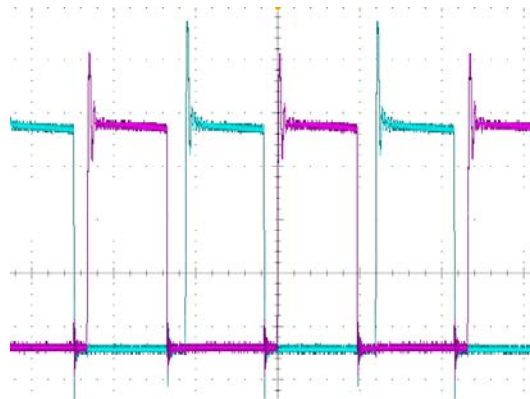


Figure 11 Effect of the snubber in V_{DS} voltages spikes.

Once the snubber is working correctly, the nominal voltage is used in the input of the converter. Figure 12 shows the V_{DS} signals and the current through the inductor. It can be distinguished that the voltage reached 500 V, there are admissible voltage surges and the overlapping time is symmetrical. Moreover, it is observed that the current has the expected behavior, is charged when both MOSFETs are on and is discharged otherwise.

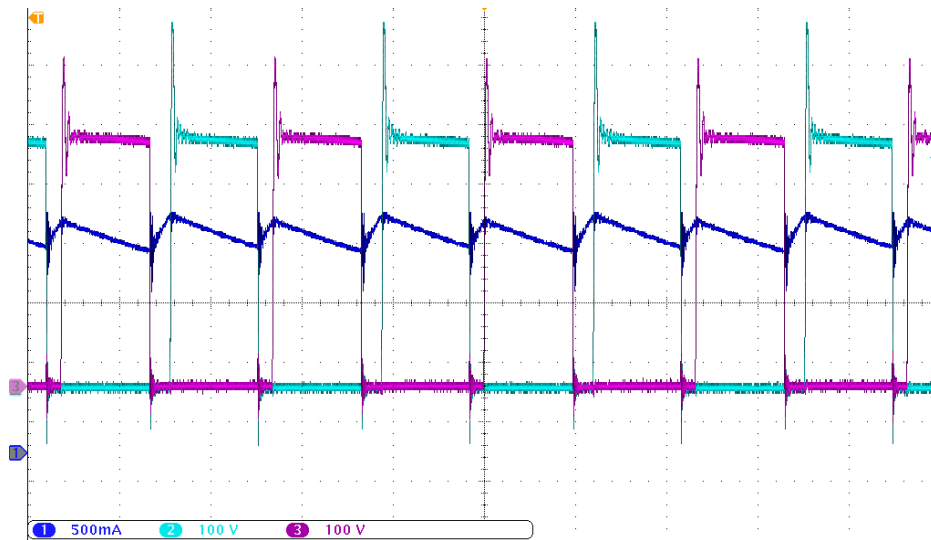


Figure 12 V_{DS} voltage from the MOSFETs (light blue and pink) and current through the inductor (deep blue).

Once there are correct signals in the input stage of the converter, the output signal is checked. Figure 13 shows the behavior of the voltage at the output of the converter. As expected, this signal is quite noisy due to the ESR of the capacitor and the inherent commutations of the converter. For this measurement, an isolated oscilloscope tip was used, so the value of Volts / div does not correspond to reality. In this case each division is equivalent to 10 V. As you can see the signal has peaks, which causes to reach 15 V to 65 V. This is unacceptable for an output of a switched power supply, so it was proceeded to construction of the output filter.

The output filter is designed as described in the previous section. The value of L obtained was 33.76 μH , while the capacitor was 300 nF. Figure 14 shows the effect of this filter on the output signal. It can be seen that the quality of the signal is

increased considerably. Now the presence of a ripple voltage is clearer. However, when analyzing the frequency of this ripple voltage it is at 120 Hz, so this is introduced by the capacitor of the input stage. To reduce it, the capacitance value must be increased. In this way, an output voltage with an admissible quality for this type of converters is presented.



Figure 13 Output voltage without LC filter.



Figure 14 Output voltage with LC filter.

4. Conclusions

This presents in detail practical considerations that must be taken into account for the construction of a current-fed push-pull DC-DC converter. An input stage, the converter design and prototypal realization have been carried on according to specifications from the output DC bus needed. Simulations confirmed performances of the whole system with protections, rectification, magnetic devices, converter, snubbers, control circuit and its initials conditions for power supply and the output filter. A 300-W prototype was developed and was accomplished an experimental testing. As further work, this converter can be done with closed loop control.

5. Bibliography and References

- [1] M. Shoyama and K. Harada, Dynamic characteristics of the Push-Pull DC to DC converter, IEEE Trans. Power Electron., vol. PE-1, pp. 3-8, 1986.

- [2] M. Shoyama and K. Harada, Steady state characteristics of the Push Pull DC to DC converter, *IEEE Trans. Aerosp. Electron. Syst.*, vol. ES-20, pp. 50-56, 1984.
- [3] Ananda and B. M. Madhu, Pre-regulated current fed push pull converter for hybrid energy systems, *Int. Conference on Computation of Power, Energy Inform. and Commun.*, Chennai, 2016, pp. 566-571.
- [4] Y. Kim, S. Shin, J. Lee, Y. Jung and C. Won, Soft-switching current-fed push-pull converter for 250-W AC module applications, *IEEE Trans Power Electron.*, vol. 29, no. 2, pp. 863-872, Feb. 2014.
- [5] A. L. Rabello, C. A. Marcio, G. C. D. Sousa and J. L. F. Vieira, A fully protected push-pull current-fed DC-DC converter, *Proc. 23rd Int. Conference on Ind. Electron., Control, and Instrumentation*, New Orleans, LA, 1997.
- [6] D. Maiti, N. Mondal, and S. K. Biswas, Design procedure of a push pull current-fed DC-DC converter, 2010.
- [7] D. Hart, DC Power Supplies, in *Power Electronics*, 1st. ed. New York, Mc.Graw-Hill, 2011.
- [8] R. Lee Ozenbaugh, *EMI filter design vol. 2*. Hesperia, California, 2001
- [9] W. T. McLyman, *Transformer and Inductor Design Handbook*. New York: Marcel Dekker, 2004.
- [10] ANSYS Maxwell, Maxwell Online Help, ANSYS, Feb. 2017: www.support.ansys.com.